Notice of Allowability	Application No.	Applicant(s)	
	09/870,447	BOLES ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *29 September 2004*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ The drawings filed on *24 September 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 20040929; 20041025
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 29 September and 25 October 2004 have been considered by the Examiner.

2. On the IDS of 29 September 2004, the Applicant listed the following prior art previously cited by the Examiner: "Z80 Family Interrupt Structure" by M. Moore, US Patent Number 5,056,004 to Ohde et al., US Patent Number 5,740,451 to Muraki et al., US Patent Number 5,826,072 to Knapp et al., US Patent Number 5,875,342 to Temple, US Patent Number 5,937,199 to Temple, US Patent Number 6,084,880 to Bailey et al., US Patent Number 6,181,151 to Wasson, and US Patent Number 6,260,162 to Typaldos et al. These references have been considered by the Examiner. However, to avoid confusion in the publication process, these references have been crossed out and indicated as a duplicate on the IDS.

3. The information disclosure statement filed 29 September 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. Applicant has submitted

foreign references Q, R, S, T, and U of Page 1 and U of Page 2; non-patent references V, W, and X of Page 1 and W, X, and Y of Page 2; and PCT Search Reports D and U of Page 3 and Y of Page 4 on a CD-ROM. In accordance with 37 CFR 1.58(e)(1), the only documents which may be submitted to the Office on a compact disc are (i) a computer program listing; (ii) a "Sequence Listing"; or (iii) a table that has more than 50 pages of text.

Allowable Subject Matter

4. Claims 1-21 are allowed. The Examiner has considered the references identified on the extensive information disclosure statements submitted on 29 September and 25 October 2004. The Examiner believes the references to be cumulative and does not believe that the references anticipate or suggest the invention as claimed. For example, US Patent Number 6,356,970 to Killian et al. teaches an interrupt control module; US Patent Number 6,295,974 to MacDonald teaches interrupt handling; US Patent Number 5,875,342 to Temple teaches a programmable interrupt mask; and US Patent Number 5,611,061 to Yasuda teaches interrupt processing. The Examiner could find neither prior art cited in its entirety nor motivation to combine the prior art to construct the invention as claimed. Should Applicants be aware of any portions of the references believed to be related to the patentability of the present application, they are reminded to notify the Examiner in accordance with 37 CFR 1.313 and MPEP §1308.

5. In reference to independent claim 1, the prior art of record fails to teach a method of processing an interrupt disable instruction included in a program instruction sequence, comprising: fetching an interrupt disable instruction from the sequence including an operand specifying a number of cycles for disabling interrupt processing; and executing the instruction. In reference to independent claim 14, the prior art of record fails to teach a processor including an interrupt disable instruction processing feature, comprising: a program memory for storing instructions including an interrupt disable instruction having an operand specifying a number corresponding to an interrupt disable duration; a register for storing the number; an instruction fetch/decode unit for fetching and decoding instructions, the instruction fetch/decode unit decoding the interrupt disable instruction and disabling the interrupt processing capability of the processor based on the number.

6. The most relevant prior art found by the Examiner is US Patent Number 6,084,880 to Bailey et al. ("Bailey"), US Patent Number 5,875,342 to Temple ("Temple-342"), US Patent Number 5,937,199 to Temple ("Temple-199"), US Patent Number 5,740,451 to Muraki et al. ("Muraki"), and Z80 Family Interrupt Structure ("Z80"). Bailey teaches disabling interrupts by setting a bit in an interrupt enable register for a period of time specified in a register (See Figures 7 and 8 and Column 15 Lines 14-41). Bailey does not teach fetching an interrupt disable instruction that includes an operand for specifying a number of cycles for disabling interrupt processing. Temple-342 and Temple-199 both teach an instruction that disables interrupts for a period of time

specified in a register. Temple-342 and Temple-199 do not teach that the period of time is specified by an operand included in the interrupt disable instruction (See Abstract). Temple-342 and Temple-199 further teach that the value representing the length of time that interrupts are disabled should be fixed by the system and not be made available to the user to ensure that the timeout period is not altered to an abnormally long period of time, which would undermine the utility of coupling the interrupt mask with a timeout counter (See Column 8 Lines 21-29). Muraki teaches a counter that measures the maximum amount of time that interrupts are disabled while a program is running (See Abstract and Column 2 Line 27 – Column 3 Line 24). Muraki does not teach fetching an interrupt disable instruction that includes an operand for specifying a number of cycles for disabling interrupt processing. Z80 teaches the use of an instruction to disable interrupts. However, Z80 requires the use of an enable interrupt instruction to enable interrupts following a disable interrupt instruction. Z80 does not provide for an operand in the instruction indicating the length of time that the interrupts are to be disabled. Thus, the prior art of record is not seen to teach or suggest the invention in the combination as claimed.

7. The Examiner has interpreted the claims in light of the enabling specification (See Figures 3 and 4 and Page 9 Line 19 – Page 13 Line 2) in view of Applicant's persuasive arguments in the response of 22 April 2004 at Pages 4-6, and therefore finds that the claims are in condition for allowance.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

TJC

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